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FM0/MANCHESTER ENCODING USING SOLS TECHNIQUE BY THE IMPLEMENTATION OF LOW POWER FOR DSRC APPLICATION

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Abstract- The Dedicated Short Range Communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding diversity between the FM0/Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. Here the Similarity Oriented Logic Simplification (SOLS) technique is proposed to overcome this limitation.

Dedicated Short-Range Communications are one-way or two-way short-range to medium-range wireless communication channels specifically designed for automotive use and a corresponding set of protocols and standards. In telecommunication and data storage, Manchester coding (also known as Phase Encoding, or PE) is a line code in which the encoding of each data bit has at least one transition and occupies the same time. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc-balance and are widely adopted in encoding for downlink. The Manchester encoding is realized with a XOR operation for CLK which has a transition within one cycle and input X.

The hardware architecture of FM0 encoding should start with the FSM of FM0 first. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, and enhances the signal reliability. The coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation, which improves the hardware utilization rate. In this project Xilinx-ISE tool is used for simulation, logical verification, and further synthesizing. In this paper the sparse kogge implementation results less area and reduced power than the existing kogge implementation.

KEYWORDS: FM0, MANCHESTER, SPARSE KOGGE, KOGGE

I. INTRODUCTION

DSRC is a protocol and is commonly known as dedicated short range communication which is utilized for medium range communication for one or two way. There are two general categories of DSRC which are mentioned below:

i) Automobile to automobile
ii) Automobile to roadside.

In the automobile to automobile the message sending will be enabled by DSRC and is among the automobiles it is broadcasted. On the other hand, the intelligent transportation services are focused in auto mobile to roadside DSRC and these include ETC (electronic toll collection). There is a possibility of a transceiver in DSCR and it consists mainly of a processing which is baseband, microprocessor as well as RF front end. In order to transfer the instruction to the baseband processing and RF front end, the microprocessor will be used.

The arbitrary binary sequence is present in the signals which are transmitted and dc balance achievement is a difficult task. The transmitted signals are initially provided by fm0 and Manchester which later on provide the dc balance. There are two methods in SOLS (known generally as Similarity Oriented Logic Simplification). ACR (Area Compact Retiming) and BOLS (the Balance Logic Operation Sharing) are two methods.

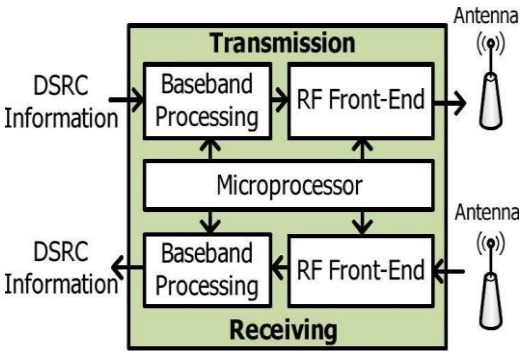

Fig.1. System Architecture of DSRC Transceiver.

The coding principles of FM0 and Manchester codes gives a limitation analysis on hardware utilization of FM0 and Manchester encoders. This section shows the difficulty to design a fully reused VLSI architecture for FM0 and Manchester encoders. The proposed VLSI architecture design using SOLS technique is reported. Two core methods of SOLS technique, area compact retiming and balance logic-operation sharing, are described in this section. The experiment results and discussion are presented. This section focuses on an objective evaluation between this design and existing articles of Manchester and FM0 encoders.

II. EXISTING METHOD

1. PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

1.1. FM0 Encoding

There are three main rules of fm0 encoding:

- If 0 is the logic for X, the fm0 code contains the transition between A and B
- If 1 is the logic for X, in between A and B no transition will ever be allowed.
- In each code for fm-0 the transition is allocated.

The following diagram shows the wave form. Clock is there inside the fm0 and also the x. there are clocks and cycles having cycles in all the transactions.

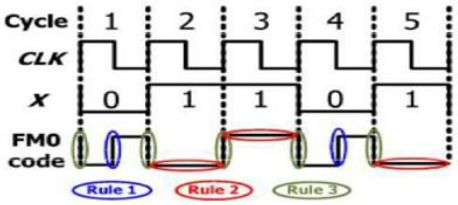

Fig.3. FM0 Encoding

1.2. Manchester Encoding

With the help of XOR operations, the Manchester encoding is realized and is actually utilized for X and the clock. The clock within one cycle always has a transition.

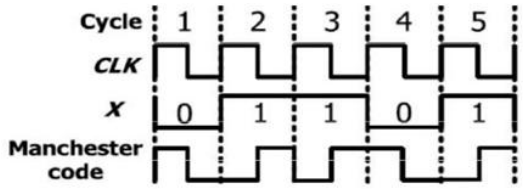

Fig.3: Manchester Encoding

2. THE STATE CODE PRINCIPLE FOR FM0/MANCHESTER ENCODING

XOR operation and Manchester encoding is the same thing. With the principle of FSM the FM0 code is supposed to start. There are four states of FSM and Fm0 code. The figure below represents these codes.

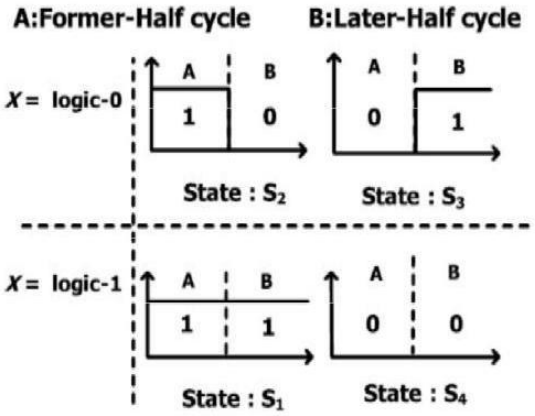

Fig.4:FSM of FM0

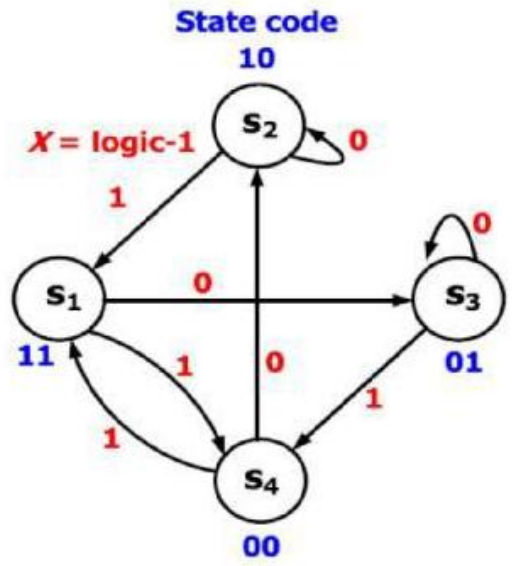

Fig.5:State diagram

If the S1 is the initial state and 11 is the code for this state for both A and B respectively. If X is at logic 0, both rules for FM01 and 3 are supposed to be followed by state transition. The next state in the only one is likely to fulfill both the rules for X and s3 is the logic 0. If logic 1 is there with X the FM0 and 3 rules are supposed to be followed by state transition. To satisfy both rules for the X of logic-1 is S4 the only one next state is there. Hence we can say that, for each of the state, the state transition can be constructed completely.

3. REVIEW OF VLSI ARCHITECTURES FOR

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FM0 ENCODER AND MANCHESTER ENCODER

For optical communications we have suggested the Manchester encoder's VLSI architecture. The CMOS inverters will be adopted by these designs and as a switch to construct are the gated inverters. 0.35-μm CMOS technology is used to implement it and 1 GHz is generally the operational frequency. Furthermore the literature offers the replacement of switch architecture by the device known as nomos. In the CMOS technology for 90-nm the maximum value for the frequency of operation is as much as 5GHz.

With Manchester and Miller encodings for radio frequency identification (RFID) applications the developing of a high-speed VLSI architecture will almost fully reused. The maximum operation frequency will be 200 MHz and the design is realized by using 0.35-μm CMOS technology.

III. IMPLEMENTATION METHODOLOGY

1. THE SUGGESTED METHODOLOGY

The coding variation and diversity between the two is likely to restrict the VLSI design potential and they can be totally refused with each other. With the help of similarity oriented logic simplification here we can propose a VLSI architectural design and there are two core methods used in this technique and they are as follows:

i) Area compact retiming

ii) Balance logic operation sharing.

The relocation of hardware to reduce 22 transistors is done by area compact retiming.

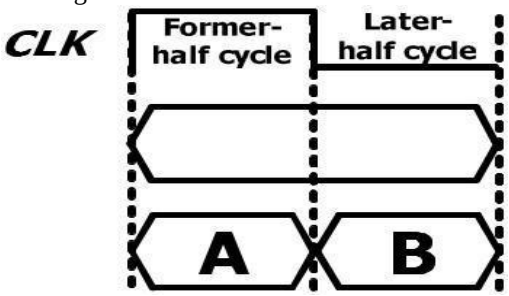


Fig.6: Code Word Structure of FM0

On the other hand, the FM0 and Manchester encodings are successfully combined with the help of balance logic operation sharing along with the hardware architecture which is reused fully. With the help of a technique known as SOLS, the VLSI which is fully reused can be constructed for the Manchester architecture and the encodings of FM0 for the applications of DSRC. An efficient performance compared with sophisticated works is achieved by the designs is revealed in the outcomes of these experiments.

2. FMO & MANCHESTER ENCODER USING SOLS TECHNIQUE

Area compact retiming (ACR) and Balance logic operation sharing (BOLS) are the two important parts of SOLS technique.

2.1.The ACR or (Area Compact Retiming)

DFFA and DFFB are used for the storage of each state for fm0. the previous state of B(t-1) determines the transition of the state code instead of the two A(t-1) and B(t-1).

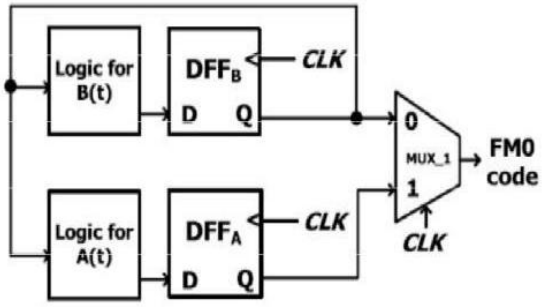


Fig.7: Area Compact Retiming

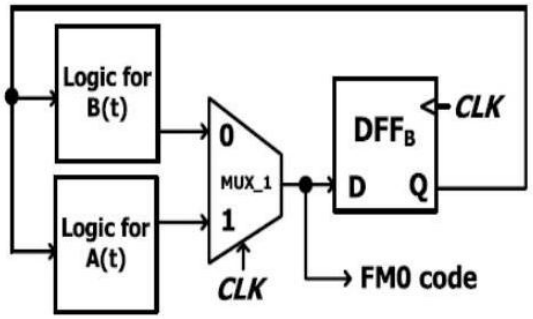


Fig.8: without Area Compact Retiming

A(t-1) and then the B(t-1) are used to represent the previous states and A(t) and then the B(t) are used to represent the current state.

Therefore, single 1-bitflip-flop to store the previous value B(t−1) is required by FM0 encoding. A fault of fm0 code is caused if the DFFA is directly removed, a non synchronization between A(t) and B(t). in order to overcome such kind of faults, right after MUX-1 the DFFB is relocated right after it. It is also assumed that DFFB is at the positive-edge triggered flipping flop. For FM) code, at each cycle the A and B are derived from the A(t) and B(t) logic respectively. Through the MUX−1 by the control signal of the CLK. the FM0 code is alternatively switched between A (t) and B (t).

In the DFFB, the Q is updated directly from the logic of B(t)with 1-cycle latency. The

B(t) will be passed through MUX−1 to the D of DFFB especially when CLK is logic 0. At this time, the next coming CLK's positive edge is updated to Q of DFFB. The diagram timing for Q of DFFB is seen with high consistency regardless of the matter if DFFB is relocated or not.

Whether the DFFB is relocated or not the timing diagram for the Q of DFFB is consistent. FM0 encoding architecture in the transition count lacking area compact retiming is 72 and if area compact retiming is there its value is 50. 22 transistors therefore are required by area compact retiming.

2.2 Balance Logic Operation Sharing(BOLS)

Using the XOR operation the Manchester encoding is derived.To integrate the X into A(t) and B(t) is the main concept of balance logic operation sharing. common point of the multiplexer like logic with the selection of the CLK are there in the fm0 and Manchester logics and below this topic the balance logic operation sharing's diagram is mentioned.

From an inverter of B(t − 1), the A(t) can be derived and by an inverter of X the value of X is obtained. The a multiplexer is placed before the inverter to switch he operands of B(t − 1) and X and the logic for A(t)/X can share the same inverter. It is also indicated in the mode that any of the fm0 or Manchester encoding is adopted. To the logic for B(t)/X the similar concept can be applied as well.

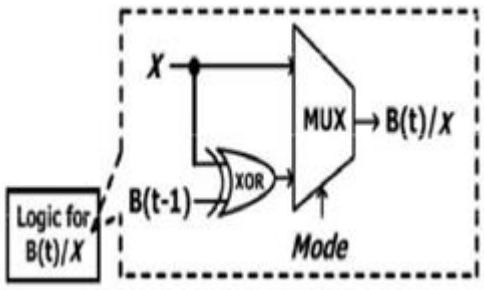


Fig.9: Balance Logic Operation Sharing.

The architecture of the balance computation time between A(t)/X and B(t)/X is used to alleviate this lack of balance between the computation time, the XOR which is in the logic for B(t)/X had translated into the XNOR along with an inverter, and then this inverter is shared with that of the logic for A(t)/X. To the output of MUX−1 this shared inverter will be relocated in the backward direction and therefore the computation logic and the time between A(t)/X and B(t)/X are in more balance.

2. HARDWARE ARCHITECTURE OF FM0/MANCHESTER ENCODER

The hardware architecture of the fm0/Manchester code is described completely in this section. In this the then the bottom part is denoted as the Manchester code and the top part is denoted the fm0 code. To store the state code of the fm0 code and also mux_1 in fm0 code the DFFA and DFFB are used. Also in fm0 code no gates are used.

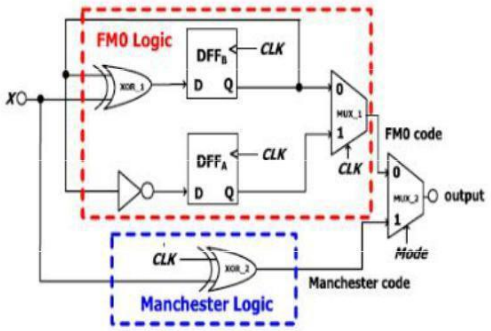


Fig.10:Hardware Architecture

When the mode=0 is given for the fm0 code. By using the XOR gate the Manchester code is developed.

The components which work with both Manchester code and fm0 are considered as active components. The number of the components which are present in the whole circuit determines the total number of components. In the following section the HUR rate is mentioned.

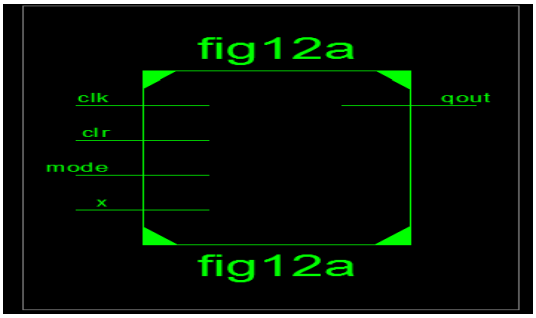
7 is the number of components for both methods of encoding also the total components are 7 for fm0 code and the Manchester code consists of 6 components which has total number of seven components out of which 2 are considered as active components in both coding with 98 transistors without the use of SOLS technology. There are 86 transistors in fm0 and there are 26 transistors in Manchester and 56 transistors is the average for both codlings.

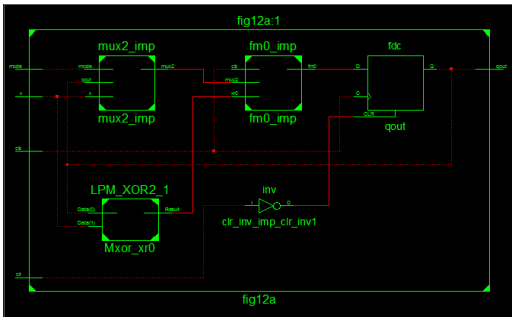
In the work mentioned here, there is a reduction of number of components from seven to six and therefore this is also a reduction in the count of transistors. two multiplexer is used in the proposed work are used in this paper which lessen the two multiplexer from one multiplexer. As the multiplexers are reduced there is also a reduction of net number of area components and hence, power consumption and the area are also reduced further.

IV. SIMULATION RESULTS

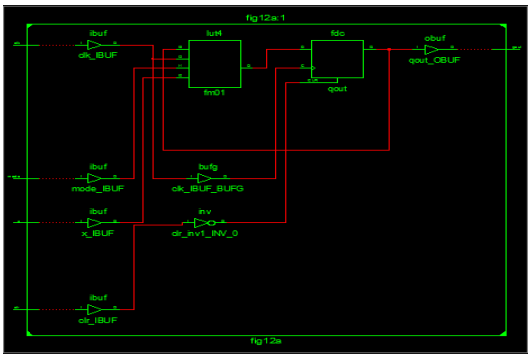
7.1.

7.2. **A. SCHEMATIC SYMBOL**

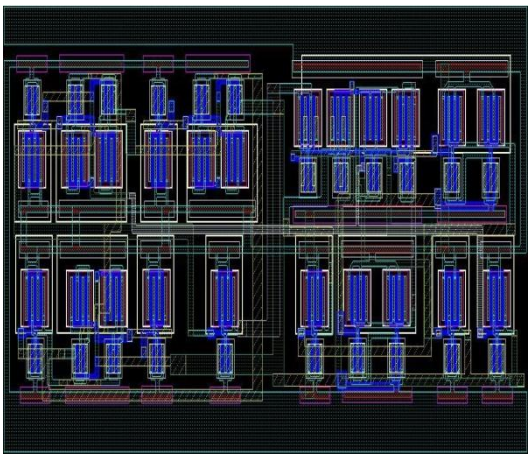




B. TECHNOLOGY SCHEMATIC



C. LAYOUT REPRESENTATION



V. CONLCUSION

The diversity of coding in the Manchester encodings and FM0 results in certain hardware utilization restrictions for the VLSI architectural design. For FM0 and Manchester encoding the analysis limitation is elaborated and discussed in details here. The fully reused VLSI architecture using SOLS technique in this paper is proposed for both Manchester encodings and Fm0. Two core techniques are there to eliminate the limitation of hardware utilization with the help of SOLS technique and these are balance logic operation sharing and area compact retiming. Fm0 and Manchester encodings are efficiently combined by the balance logic operation sharing with the similar factors in the logic components. In this case, it is made possible with the help of Cadence Virtuoso.

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